sddec23-08

ReRAM Compute ASIC Fabrication

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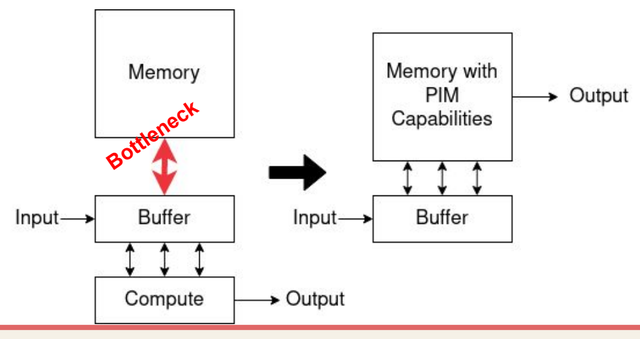
Intro/Motivation

- Implement an 8x8 ReRAM crossbar in the SkyWater 130 nm process
- In memory computing eliminates memory bottlenecks, increasing computation speed
- Contribute towards Iowa State's institutional knowledge of eFabless chip fabrication
- Contribute towards ReRAM research



Users

- Future students interested in analog ASIC design
- Dr. Duwe
  - Wants to develop in house ISU computational ASIC capabilities
- Dr. Wang
  - Interested in ReRAM computation and fabrication

Process Flow

Designing all of our components using open-source tools is required in the analog process flow for eFabless chip fabrication.

Tool	Function
Xschem	Circuit Editor
Ngspice	Spice Simulator
Magic	Layout & DRC
Netgen	LVS

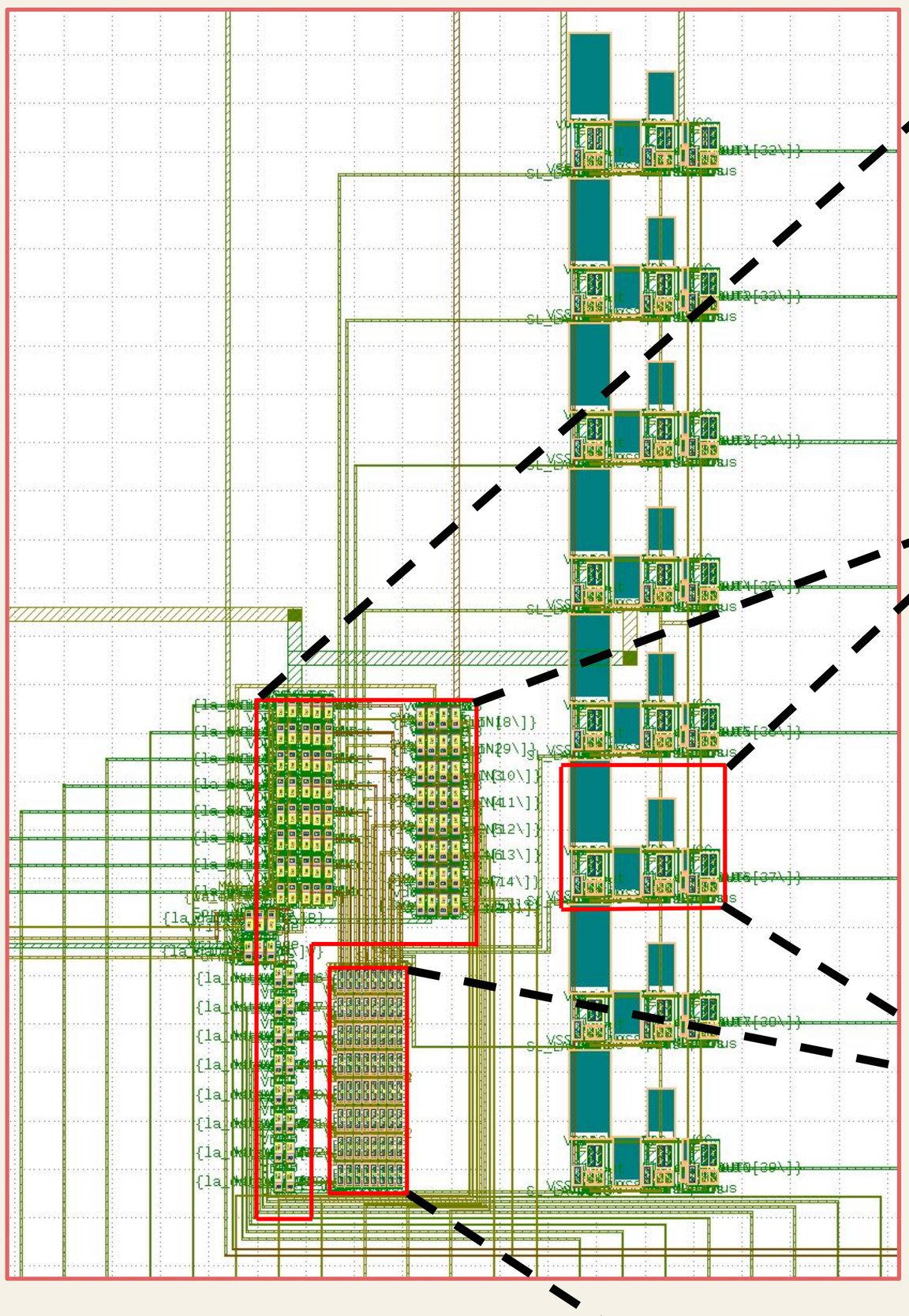
Xschem → Ngspice → Magic → Netgen → Ngspice

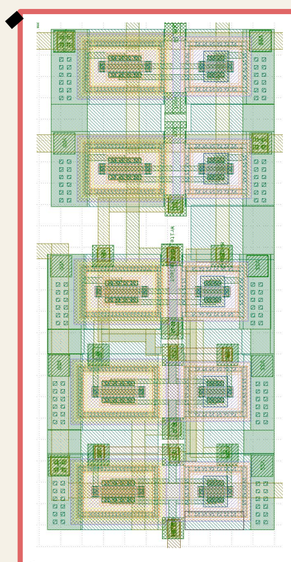
Design Requirements

- 8x8 ReRAM crossbar can perform write, read, & MAC operations
- Create periphery analog circuitry to support crossbar computations
- Usage of 1T1R storage cell
- Crossbar must output high whenever a single storage cell is in a LRS (low resistive state)
- Interface with the ReRAM compute crossbar using the Caravel Harness
- Design must fit in user project area (10 mm^2)
- Design must pass the eFabless pre-check
- Create tutorial documentation on open-source analog design flow

Engineering Standards

- IEEE 1364-2005 : Verilog
- ISO/IEC 9899:2011 : C11
- IEEE 1149-2010 : Mixed Signal Test Bus



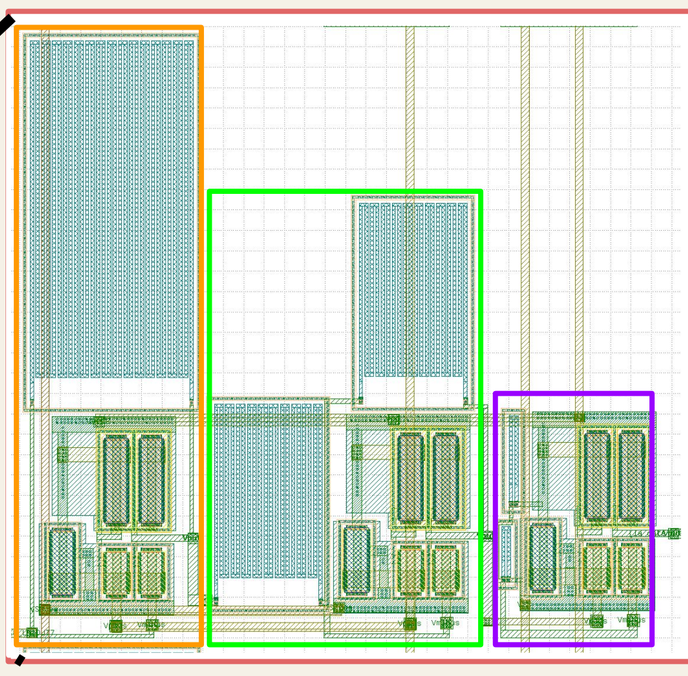


Input Voltage Shifters

We have 3 blocks of input voltage shifters corresponding to each input. We have 3 different inputs to the crossbar:

- Bitline
- Sourceline
- Wordline

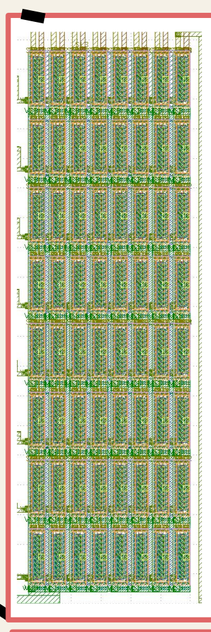
Each input needs a different voltage to operate the 1T1R cells.



Output Pipeline

Pipeline necessary to convert output currents into usable output voltages. Contains 3 stages:

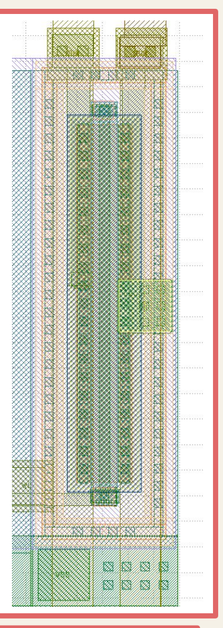
1. TIA (I -> -V)
2. Inverting Amp (-V -> V)
3. ADC (AV -> DV)



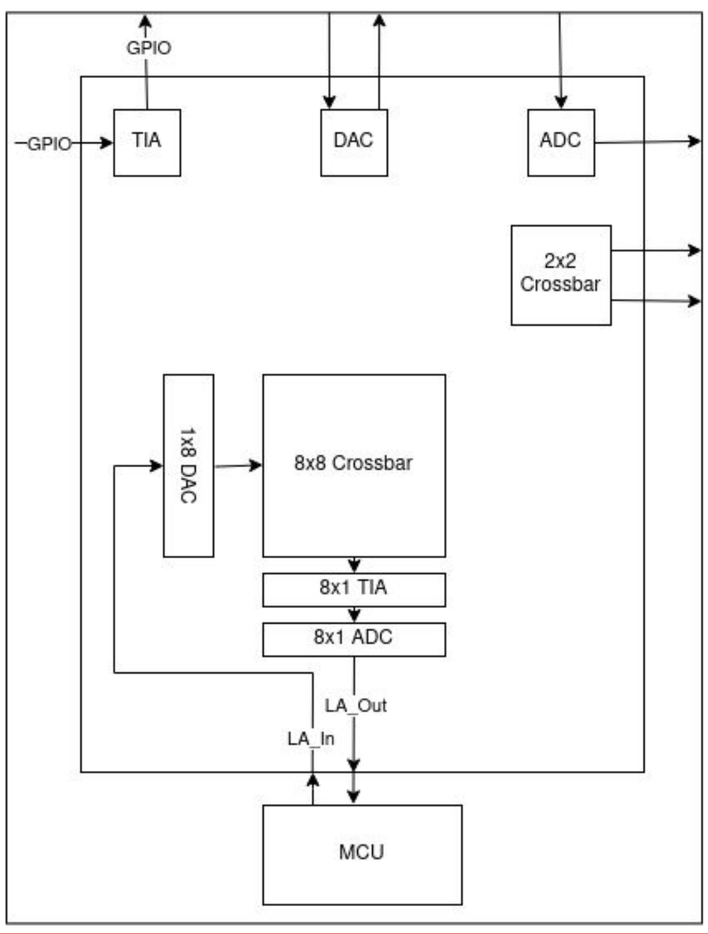
ReRAM Crossbar

8x8 Crossbar of 1T1R cells. Is able to do multiply and accumulates by summing currents along it's column.

1T1R Cells contain one ReRAM cell and 1 transistor. It stores a value of '1' when its conductance is high, and '0' when it's conductance is low.



Concept Sketch



Testing

Unit Testing

- Schematic simulations
- Post-layout R+C simulations

System Testing

- Corner and error testing of top-level design

Results

Our testing has shown the 8x8 compute crossbar we designed works within expected error margins.

# of cells in LRS	# of cells in HRS	TEST	BL_In (V)	SL_In (V)	InvOut (V)	Vout (V)
0	8	TT	0.1879	0.0592	0.4692	0.0057
0	8	SS	0.1847	0.0578	0.4557	0.0039
0	8	FF	0.1901	0.0602	0.4795	0.0077
1	7	TT	0.1804	0.1203	0.7049	1.784
1	7	SS	0.1749	0.1147	0.7064	1.787
1	7	FF	0.1846	0.1245	0.7057	1.778